

CLAIMS

What is claimed is:

- 1 1. An execution unit in a microprocessor, the execution unit comprising:
 - 2 look-up memory; and
 - 3 a first circuit coupled to the look-up memory,
 - 4 the first circuit, in response to the microprocessor receiving a first
 - 5 instruction, partitioning the look-up memory into a first
 - 6 plurality of look-up tables,
 - 7 the first circuit, in response to the microprocessor receiving a second
 - 8 instruction, partitioning the look-up memory into a second
 - 9 plurality of look-up tables which are different from the first
 - 10 plurality of look-up tables.
- 1 2. An execution unit as in claim 1 wherein a total number of bits used by each entry in the first plurality of look-up tables is different from a total number of bits used by each entry in the second plurality of look-up tables; and wherein the microprocessor is a media processor formed in a monolithic semiconductor substrate, which comprises a memory controller for controlling DRAM memory, said media processor being coupled to said memory controller.

- 1 3. An execution unit as in claim 1 wherein a total number of entries in each of
2 the first plurality of look-up tables is different from a total number of entries
3 in each of the second plurality of look-up tables.

- 1 4. An execution unit as in claim 1 wherein the look-up memory comprises a
2 plurality of look-up units, and wherein the first circuit configuring the
3 plurality of look-up units into a third plurality of look-up tables in response
4 to the microprocessor receiving a third instruction.

- 1 5. An execution unit as in claim 4 wherein each of the third plurality of look-up
2 units contains 256 8-bit entries.

- 1 6. An execution unit as in claim 4 wherein a total number of entries in each of
2 the third plurality of look-up tables is one of:
3 a) 256;
4 b) 512; and
5 c) 1024.

- 1 7. An execution unit as in claim 4 wherein a total number of bits used by each
2 entry in the third plurality of look-up tables is one of:
3 a) 8;
4 b) 16; and

5 c) 24.

1 8. An execution unit as in claim 1 further comprising:
2 a second circuit coupled to the look-up memory, the second circuit
3 configured to receive a plurality of numbers, in response to the
4 microprocessor receiving the first instruction, the first plurality of
5 look-up tables looking up simultaneously a plurality of entries, each
6 of the plurality of entries being in one of the plurality of look-up
7 tables and being pointed to by one of the plurality of numbers.

1 9. An execution unit as in claim 1 further comprising:
2 a second circuit coupled to the look-up memory, the second circuit
3 configured to receive a string of bits, in response to the
4 microprocessor receiving the first instruction,
5 the second circuit generating a plurality of indices using a plurality of
6 segments of bits in the string of bits,
7 the first plurality of look-up tables looking up simultaneously a plurality of
8 entries, each of the plurality of entries being in one of the plurality of
9 look-up tables and being pointed to by one of the plurality of indices.

1 10. An execution unit as in claim 9 further comprising:
2 a third circuit coupled to the look-up memory, the third circuit combining the
3 plurality of entries into a first result.

- 1 11. An execution unit as in claim 10 further comprising:
 - 2 a forth circuit coupled to the second circuit, the forth circuit configured to
 - 3 receive a plurality of data elements specifying the plurality of
 - 4 segments in the string of bits.
- 1 12. An execution unit as in claim 10 further comprising:
 - 2 a fifth circuit coupled to the second circuit, the fifth circuit configured to
 - 3 receive at least one format; and
 - 4 a sixth circuit coupled to the fifth circuit and the third circuit, in response to
 - 5 the microprocessor receiving the first instruction,
 - 6 the fifth circuit formatting the string of bits into at least one escape data using
 - 7 the at least one format, and
 - 8 the sixth circuit combining the at least one escape data with the first result
 - 9 into a second result.
- 1 13. A processing system comprising an execution unit as in claim 1.
- 1 14. A microprocessor execution unit comprising:
 - 2 a plurality of look-up tables;
 - 3 a first circuit configured to accept a first plurality of numbers, each of the
 - 4 first plurality of numbers pointing to one of a plurality of entries, each

5 of the plurality of entries being in one of the plurality of look-up
6 tables
7 a second circuit configured to accept a second plurality of numbers; and
8 a third circuit coupled to the first circuit, the second circuit, and the plurality
9 of look-up tables, the third circuit, in response to the microprocessor
10 receiving a single instruction, replacing simultaneously the plurality
11 of entries in the plurality of look-up tables with the second plurality
12 of numbers.

1 15. A processing system comprising an execution unit as in claim 14.

1 16. An execution unit in a microprocessor, the execution unit comprising:
2 a plurality of look-up tables;
3 a first circuit coupled to the plurality of look-up tables and a Direct Memory
4 Access (DMA) controller, the first circuit, in response to the
5 microprocessor receiving a single instruction, replacing at least one
6 entry in at least one of the plurality of look-up tables with at least one
7 data element using the DMA controller.

1 17. A processing system comprising an execution unit as in claim 16.

1 18. An execution unit in a microprocessor, the execution unit comprising:
2 a plurality of look-up tables;

3 a first circuit coupled to the plurality of look-up tables and a Direct Memory
4 Access (DMA) controller, the first circuit, in response to the
5 microprocessor receiving a single instruction, replacing at least one
6 entry for each of the plurality of look-up tables with a plurality of data
7 elements using the DMA controller.

1 19. A processing system comprising an execution unit as in claim 18.

1 20. An execution unit in a microprocessor comprising:
2 a plurality of look-up tables;
3 a first circuit coupled to the plurality of look-up tables, the first circuit
4 configured to receive a string of bits;
5 a second circuit coupled to the plurality of look-up tables and the first circuit,
6 the second circuit configured to receive a plurality of data elements,
7 in response to the microprocessor receiving a single instruction,
8 the second circuit generating a plurality of indices using the plurality
9 of data elements and the string of bits,
10 the plurality of look-up tables looking up simultaneously a plurality
11 of entries using the plurality of indices; and
12 a third circuit coupled to the plurality of look-up tables, the third circuit
13 combining the plurality of values into a first result.

1 21. An execution unit as in claim 20 further comprising:

2 a fifth circuit coupled to the second circuit, the fifth circuit configured to
3 receive at least one format; and
4 a sixth circuit coupled to the fifth circuit and the third circuit, in response to
5 the microprocessor receiving the single instruction,
6 the fifth circuit formatting the string of bits into at least one escape
7 data using the at least one format, and
8 the sixth circuit combining the at least one escape data with the first
9 result into a second result.

1 22. A processing system comprising an execution unit as in claim 21.

1 23. An execution unit in a microprocessor, the execution unit comprising:
2 means for receiving a first plurality of numbers and a second plurality of
3 numbers, each of the first plurality of numbers pointing to one of a
4 plurality of entries, each of the plurality of entries being in one of a
5 plurality of look-up tables; and
6 means for replacing simultaneously the plurality of entries in the plurality of
7 look-up tables with the second plurality of numbers;
8 wherein the above means operate in response to the microprocessor receiving
9 a single instruction.

- 1 24. An execution unit as in claim 23 wherein the first plurality of numbers are
- 2 received from a first entry in a register file; and the second plurality of
- 3 numbers are received from a second entry in the register file.

- 1 25. An execution unit as in claim 24 wherein the single instruction specifies
- 2 indices of the first and second entries in the register file.

- 1 26. An execution unit in a microprocessor, the execution unit comprising:
2 means for replacing at least one entry in at least one of a plurality of look-up
3 units in a microprocessor unit with at least one number using a Direct
4 Memory Access (DMA) controller;
5 wherein the above means operate in response to the microprocessor receiving
6 a single instruction.

- 1 27. An execution unit in a microprocessor, the execution unit comprising:
2 means for replacing at least one entry for each of a plurality of look-up units
3 in a microprocessor with a plurality of numbers using a Direct
4 Memory Access (DMA) controller;
5 wherein the above means operate in response to the microprocessor receiving
6 a single instruction.

- 1 28. An execution unit as in claim 27 wherein a single index encoded in the
- 2 instruction specifies a location of the at least one entry in the plurality of
- 3 look-up units.

- 1 29. An execution unit as in claim 27 wherein a single index encoded in the
- 2 instruction specifies a total number of the at least one entry for each of a
- 3 plurality of look-up units.

- 1 30. An execution unit as in claim 27 wherein a source address of the plurality of
- 2 numbers is specified in an entry of a register file.

- 1 31. An execution unit as in claim 30 wherein the single instruction specifies an
- 2 index of the entry in the register file.

- 1 32. An execution unit as in claim 27 wherein an identity number encoded in the
- 2 single instruction specifies the DMA controller.

- 1 33. An execution unit in a microprocessor, the execution unit comprising:
2 means for receiving a plurality of numbers;
3 means for partitioning look-up memory into a plurality of look-up tables;
4 means for looking up simultaneously a plurality of elements from the
5 plurality of look-up tables, each of the plurality of elements being in

6 one of the plurality of look-up tables and being pointed to by one of
7 the plurality of numbers;
8 wherein the above means operate in response to the microprocessor receiving
9 a single instruction.

1 34. An execution unit as in claim 33 wherein the means for receiving a plurality
2 of numbers comprises:
3 means for partitioning a string of bits into a plurality of segments to generate
4 the plurality of numbers.

1 35. An execution unit as in claim 34 wherein the single instruction specifies
2 format information in which the plurality of numbers are stored in the string
3 of bits.

1 36. An execution unit as in claim 33 wherein the look-up memory comprises a
2 plurality of look-up units, and wherein the means for partitioning look-up
3 memory comprises:
4 means for configuring the plurality of look-up units into the plurality of look-
5 up tables.

1 37. An execution unit as in claim 33 wherein the string of bits is received from
2 an entry of a register file.

- 1 38. An execution unit as in claim 37 wherein the single instruction specifies an
- 2 index of the entry.
- 1 39. An execution unit as in claim 33 further comprising:
2 means for storing the plurality of elements in an entry of a register file.
- 1 40. An execution unit as in claim 39 wherein the single instruction specifies an
- 2 index of the entry.
- 1 41. An execution unit as in claim 39 wherein the single instruction specifies
2 format information in which the plurality of elements are stored in the entry.
- 1 42. An execution unit as in claim 36 wherein each of the plurality of look-up
2 units comprises 256 8-bit entries.
- 1 43. An execution unit as in claim 33 wherein the single instruction specifies a
2 total number of entries contained in each of the plurality of look-up tables.
- 1 44. An execution unit as in claim 43 wherein the total number of entries is one
2 of:
 - 3 a) 256;
 - 4 b) 512; and

5 c) 1024.

1 45. An execution unit as in claim 33 wherein the single instruction specifies a
2 total number of bits used by each entry contained in the plurality of look-up
3 tables.

1 46. An execution unit as in claim 45 wherein the total number of bits is one of:
2 a) 8;
3 b) 16; and
4 c) 24.

1 47. An execution unit in a microprocessor, the execution unit comprising:
2 means for receiving a string of bits;
3 means for generating a plurality of indices using a plurality of segments of
4 bits in the string of bits;
5 means for looking up simultaneously a plurality of entries from a plurality of
6 look-up tables using the plurality of indices; and
7 means for combining the plurality of entries into a first result;
8 wherein the above means operate in response to the microprocessor receiving
9 a single instruction.

1 48. An execution unit as in claim 47 wherein further comprising:

2 means for receiving a plurality of data elements specifying the plurality of
3 segments in the string of bits.

1 49. An execution unit as in claim 48 wherein the plurality of data elements are
2 received from an entry in a register file.

1 50. An execution unit as in claim 49 wherein the single instruction specifies an
2 index of the entry in the register file.

1 51. An execution unit as in claim 48 further comprising:
2 means for receiving a bit pointer, wherein the plurality of segments in the
3 string of bits are determined using the bit pointer and the plurality of
4 data elements.

1 52. An execution unit as in claim 51 further comprising:
2 means for generating a new bit pointer using the first result.

1 53. An execution unit as in claim 47 further comprising:
2 means for receiving an offset, wherein the plurality of indices are determined
3 using the offset and the plurality of segments of bits.

1 54. An execution unit as in claim 47 further comprising:

2 means for partitioning look-up memory into the plurality of look-up tables
3 before said looking-up.

1 55. An execution unit as in claim 54 wherein the look-up memory comprises a
2 plurality of look-up units, and wherein the means for partitioning look-up
3 memory comprises:
4 means for configuring the plurality of look-up units into the plurality of look-
5 up tables.

1 56. An execution unit as in claim 69 wherein each of the plurality of look-up
2 units comprises 256 8-bit entries. error

1 57. An execution unit as in claim 47 wherein the single instruction specifies a
2 total number of entries contained in each of the plurality of look-up tables.

1 58. An execution unit as in claim 57 wherein the total number of entries is one
2 of:
3 a) 256;
4 b) 512; and
5 c) 1024.

- 1 59. An execution unit as in claim 47 wherein the single instruction specifies a
- 2 total number of bits used by each entry contained in the plurality of look-up
- 3 tables.

- 1 60. An execution unit as in claim 59 wherein the total number of bits is one of:
- 2 a) 8;
- 3 b) 16; and
- 4 c) 24.

- 1 61. An execution unit as in claim 54 wherein the plurality of look-up tables are
- 2 configure according to an indicator in an entry in a register file.

- 1 62. An execution unit as in claim 61 wherein the single instruction specifies an
- 2 index of the entry in the register file.

- 1 63. An execution unit as in claim 47 wherein the means for combining the
- 2 plurality of entries comprises:
- 3 means for selecting a valid data from the plurality of entries.

- 1 64. An execution unit as in claim 63 further comprising:
- 2 means for generating an indicator indicating whether none of the plurality of
- 3 entries is valid.

- 1 65. An execution unit as in claim 63 wherein the valid data is selected according
- 2 to priorities of the look-up tables from which the plurality of entries are
- 3 looked up.

- 1 66. An execution unit as in claim 63 wherein the means for combining the
- 2 plurality of entries further comprises:
- 3 means for formatting the valid data according to a type of the valid data.

- 1 67. An execution unit as in claim 66 wherein the type of the valid data is one of:
- 2 a) zero fill;
- 3 b) sign magnitude; and
- 4 c) two complement.

- 1 68. An execution unit as in claim 67 further comprising:
2 means for retrieving a sign bit from the string of bits for the valid data,
3 wherein the first result is obtained by formatting the valid data using
4 the sign bit when the type of the valid data is sign magnitude.

- 1 69. An execution unit as in claim 47 wherein an entry in the plurality of entries
- 2 contains:
3 a) information indicating whether the entry is valid;
4 b) information indicating a type of the entry; and

5 c) information indicating a number of bits of a code word to be decoded.

1 70. An execution unit as in claim 47 wherein the string is received from an entry

2 in a register file.

1 71. An execution unit as in claim 70 wherein the single instruction specifies an

2 index of the entry in the register file.

1 72. An execution unit as in claim 47 further comprising:

2 means for receiving a first number indicating a position of a last bit of input

3 in the string of bit.

1 73. An execution unit as in claim 72 further comprising:

2 means for generating an indicator indicating whether any bit after the last bit

3 of input is used in obtaining the first result.

1 74. An execution unit as in claim 58 further comprising:

2 means for generating an indicator indicating whether one of the plurality of

3 segments of bits contains a predetermined code.

1 75. An execution unit as in claim 74 wherein the predetermined code represents

2 an end of block condition.

1 76. An execution unit as in claim 47 further comprising:
2 means for receiving at least one format;
3 means for formatting the string of bits into at least one escape data according
4 to the at least one format; and
5 means for combining the at least one data and the first result into a second
6 result.

1 77. An execution unit as in claim 76 wherein one of the at least one format is for
2 data of a type which is one of:
3 a) zero fill;
4 b) sign magnitude; and
5 c) two complement.

1 78. An execution unit as in claim 76 wherein the at least one format is received
2 from an entry of a register file.

1 79. An execution unit as in claim 78 wherein the single instruction specifies an
2 index of the entry in the register file.